**IN THE CLAIMS**:

Please note that, pursuant to 37 CFR 1.121(c)(3), all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity and for the convenience of the Patent Office. Also attached is a version with markings to show changes made to the claims.

Please cancel claim 2 without prejudice or disclaimer.

Please amend claim 1 as set forth below.

1. (Amended) A method of forming an integrated circuit package, the method comprising:
forming a lead frame having a plurality of conductors and at least one alignment feature electrically isolated from the plurality of conductors;
coupling at least some of the plurality of conductors to a semiconductor die;
encapsulating the semiconductor die and a portion of the lead frame with an insulating material; and
removing the at least one alignment feature.

3. (Previously Amended) A method of forming an integrated circuit package, the method comprising:
providing a plurality of conductors and at least one alignment feature;
coupling at least some of the plurality of conductors to a semiconductor die; and
encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material.

4. (Previously Twice Amended) A method of forming and testing an integrated circuit package, the method comprising:
providing a plurality of conductors and at least one alignment feature;
electrically coupling at least some of the plurality of conductors to a semiconductor die;
encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material;
coupling the at least one alignment feature encompassed by the insulating material with a portion

of a testing device; and

testing the integrated circuit package through at least some of the electrically coupled conductors.

Please enter new claims 18-26 as set forth below.

18. The method according to claim 1, further comprising forming the at least one alignment feature to include at least one aperture.

19. The method according to claim 1, further comprising forming the at least one alignment feature to include a plurality of apertures.

20. The method according to claim 1, further comprising forming a separation line in the lead frame and wherein removing the at least one alignment feature further comprises removing the at least one alignment feature along the separation line.

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21. The method according to claim 20, wherein the forming a separation line in the lead frame includes perforating the separation line.

22. The method according to claim 1, further comprising forming the at least one alignment feature to include a tab.

23. A method of forming and testing an integrated circuit package, the method comprising:

forming a lead frame having a plurality of conductors and at least one alignment feature electrically isolated from the plurality of conductors;

coupling at least some of the plurality of conductors to a semiconductor die;

encapsulating the semiconductor die and a portion of the lead frame with an insulating material;

coupling the at least one alignment feature with a portion of a testing device;

testing the integrated circuit package through at least some of the electrically coupled conductors;

decoupling the at least one alignment feature from the portion of the testing device; and

removing the at least one alignment feature.

24. The method according to claim 3, further comprising forming the at least one alignment feature to include an alignment cut-out.

25. The method according to claim 3, further comprising providing a heat spreader and forming the at least one alignment feature in the heat spreader.

26. The method according to claim 3, further comprising providing a tie bar and forming the at least one alignment feature in the tie bar.